Heathkit IM-102 (also Weston 1240)

Partial Logic Description

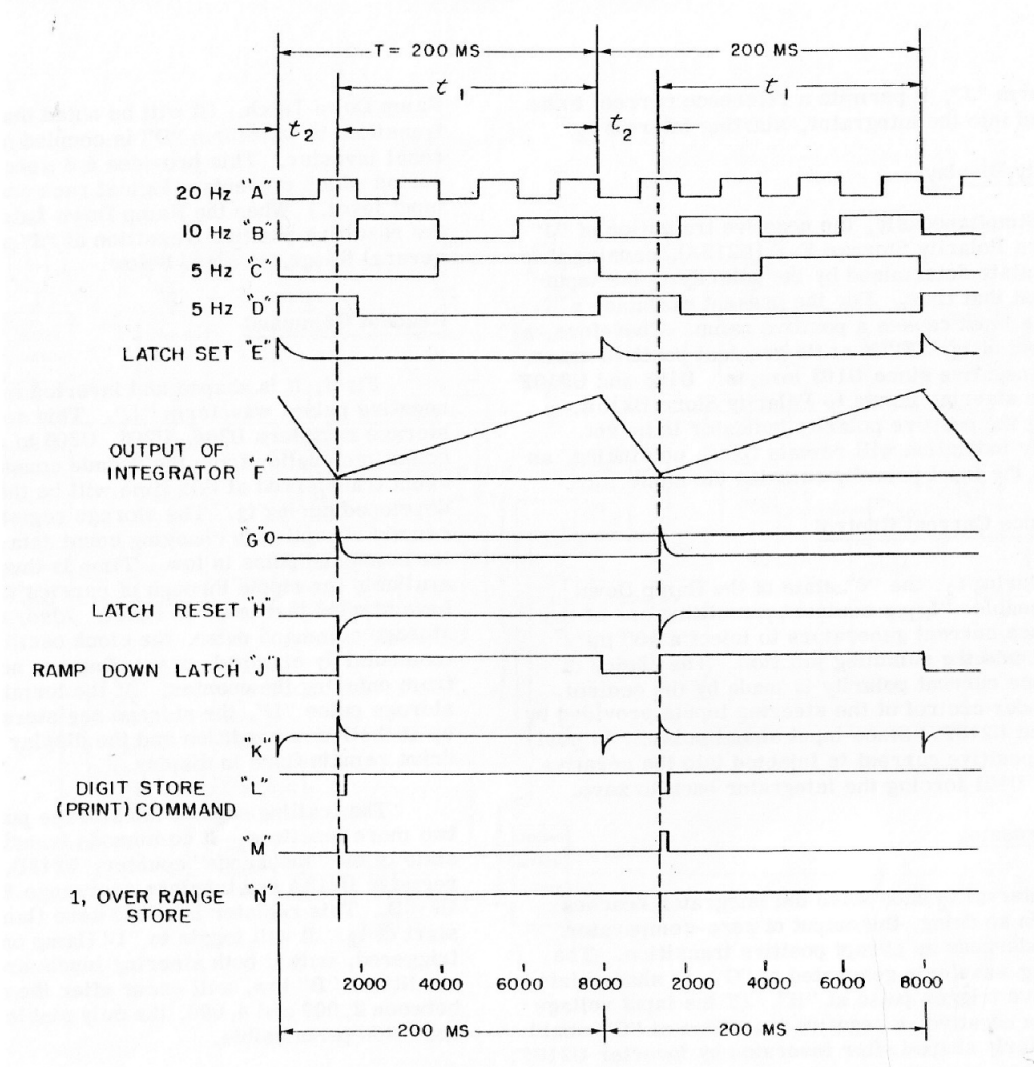
* Compiled from Heathkit and Weston circuit descriptions

* Mostly disregarding details of the dual-slope A/D Conversion & Integration

DC Voltmeter Functionality is presented (all other functions produce the same conditioned signal type & range to the A/D Converter)

See table of Heathkit/Weston logic component designations at the end of this document.

IM-102 (Weston 1240) Logic Timing Diagram *(letters correspond with logic block diagram sketch)*



The A/D Converter and the 2,000 count display (0~1999) display it generates is under control of an 8,000 count timing sequence, driven by a 40kHz clock oscillator. The clock signal drives the 8,000 step counter chain (Weston documents refer to this as an 8,000 bit counter) consisting of three decade counters IC10, IC13, IC16 and three binary dividers (flip/flops configured as divide-by-2 logic blocks) IC8B, IC5A, IC5B. The decade counters accumulate counts up to 999 and drive the three corresponding storage registers (i.e. quad latches) IC11, IC14, IC17. The three binary dividers register the 1000 count and provide 'overrange' sensing and control functions. Timing diagram waveforms for the three binary dividers (flip-flops) are assigned reference letters 'A', 'B' and 'C' in the Logic Timing diagram and also the Logic Block Diagram sketch (at the end of this document).

Synchronization

When timing waveforms 'B' and 'C' simultaneously go to logic zero, the state "8,000" is detected by logic gate IC6A. This is a reference condition which occurs only once in 8,000 clock pulses and is used to start integrator interval t_2 . In detecting 8,000, waveform 'D' goes from logic 0 to 1, a transition which sets a control register called "Ramp Down Latch" (IC6C & IC6D). [Note: the terms "Run-Up" and "Run-Down" are commonly used in descriptions of integrating A/D converters. However, Heathkit and Weston prefer "Ramp Up" and "Ramp Down", so this document uses their terminology.] The Ramp Down Latch occupies a central position in the operation of the A/D Converter. When set, producing a negative pulse waveform 'J', it permits a reference current I_{REF} to be injected into the integrator IC1, starting interval t_2 .

Polarity Display

Simultaneously, the negative transition of 'J' triggers Polarity Storage F/F (IC4A), causing it to take a state determined by the polarity of the input signal at that time. For the present example, a positive input causes a positive ramp (t_1 and t_2); a negative input signal would cause the (t_1 and t_2) ramps to be on the negative side of ground (0 Volts). Therefore, at the onset of t_2 , integrator output signal 'F' is at its greatest positive value. 'G' is negative since comparator IC3 is set up to be inverting. The comparator and inverter IC9C provide steering inputs to Polarity Store F/F (IC4A), causing the positive polarity indicator to be turned on. Polarity indication will remain fixed (by the F/F), unblinking, as long as the input polarity remains the same.

Reference Current Control

During t_2 , the "0" state of the Ramp Down Latch (IC6C & IC6D) enables "Iref Control", permitting one of the reference current generators to inject (source or sink) a 400µA current into the integrator's (IC1) summing junction; the (-) input via a 100k resistor whose presence does not affect the functionality of the integrator. The choice of which reference current polarity to use is made by the control logic (IC7A, IC7B, IC7C) under control of the steering inputs provided by the integrator's comparator (IC3) and inverter (IC9C). Since, for example, an input signal polarity is positive, a positive current is injected into the (-) input of integrator (IC1), forcing the integrator to ramp back towards zero.

Zero Crossing

Interval t_2 ends when the integrator output reaches zero (coming from either the positive or negative direction, according to the polarity of the meter input signal). In so doing, the output of the Zero Crossing Comparator (IC3) undergoes an abrupt negative to positive transition (assuming the input signal is positive and the integrator ramp has been positive). The resulting comparator output waveform 'G' is shaped into a negative trigger pulse 'H' by the Zero Crossing Shaper circuit (IC7D and its two RC conditioners). [*If the meter input voltage had been negative, a negative transition at 'G' would be similarly shaped after inversion by inverter IC9C. Therefore, any zero-crossing event is converted into a negative trigger pulse.*] The zero-crossing trigger pulse at 'H' is inverted by Reset Inverter (IC6B) and applied to reset the Ramp Down Latch (IC6C & IC6D). [*It will be noted that the positive transition of waveform 'D' is RC coupled over to the Reset Inverter. This provides a 6μS Inhibit period which prevents a logical race condition at a zero input level.*] When the Ramp Down Latch is reset, the resulting positive transition at 'J' accomplishes several things, as noted below.

Readout Command

First, 'J' is shaped and inverted into a 1μS negative pulse 'L' (by an RC pair and inverter IC9D). This 'storage pulse' commands the storage registers (IC17, IC14, IC11) to accept new count information from the decade counters. The count transferred at this time will be the number "N" developed during interval t_2 . The storage registers will remain receptive to changing count data as long as the command pulse 'J' is low (i.e. 'negative'). [*The analog circuit signals can be positive or negative, the IC3 comparator output can only be positive (due to IC3's special ground reference connection), and the logic circuit signals can only be positive. However, when referring to logic signals changing states, it is often convenient to refer to them as going positive or negative, even though they are only 'negative' relative to positive, and cannot be lower than circuit ground/zero volts.*] Time is thus made available for count-ripple-through of 'carries' (from one counter to the next) which may have started just prior to reset. Also, during the storage command pulse, the clock oscillator is momentarily clamped (via D8), preventing any new pulses from entering the counter. At the termination of storage pulse 'L', the storage registers are locked at their new condition and the display tubes they control remain fixed in their reading.

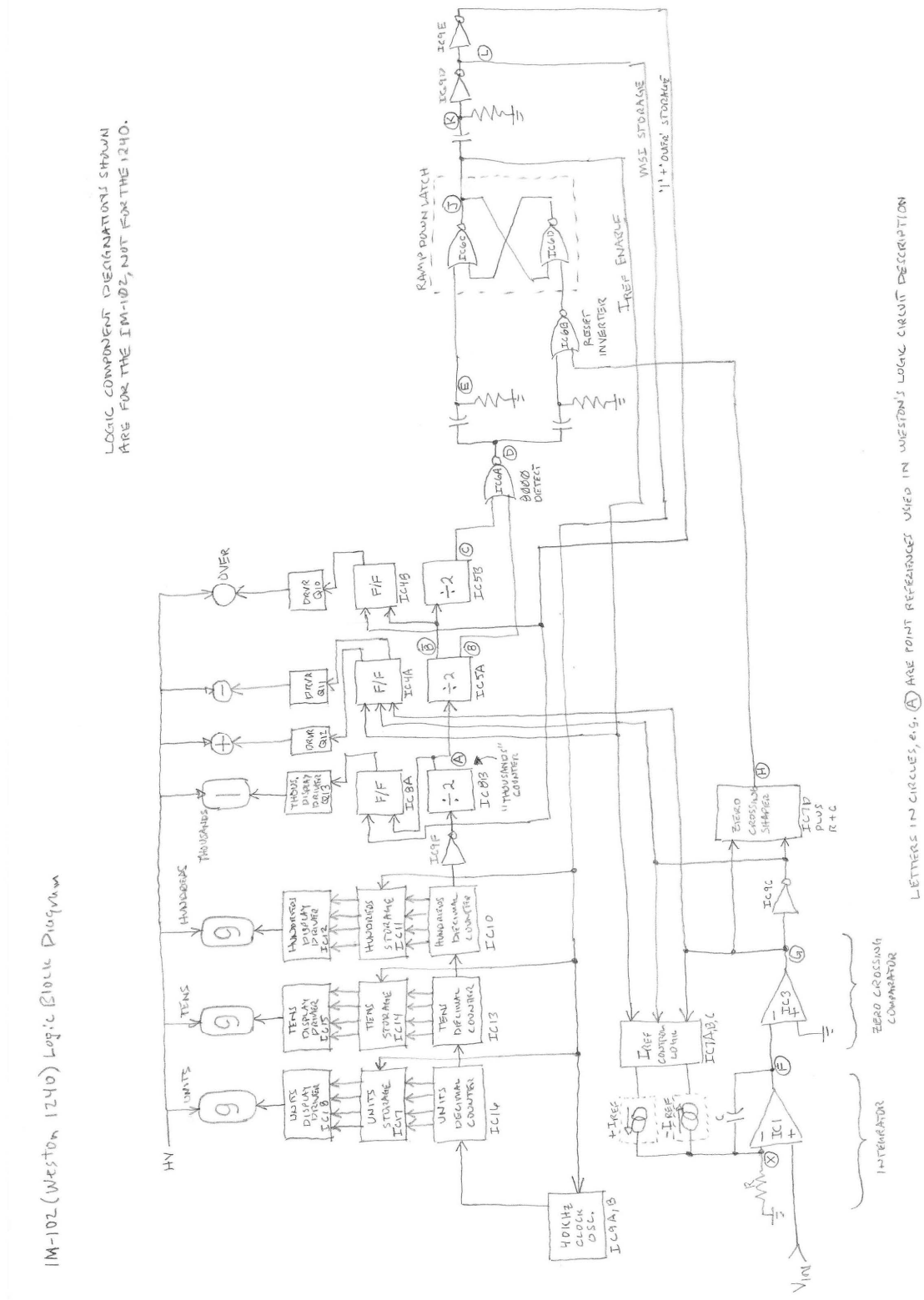
The trailing edge of the storage pulse activates two more functions. It commands transfer of the state of the "thousands" counter (F/F IC8B) into the "thousands" storage register (F/F IC8A), and it also triggers the "overrange" flip-flop (F/F IC4B). The "overrange" register is set to logic 0 (overrange lamp off) at the start of interval t_2 ; it will toggle to logic 1 (overrange lamp on) when triggered, but only if both steering inputs are logic low. This condition, 'B low' (depicted on the block diagram sketch as a B with a line over it), will occur after the count of between 2,000 and 4,000, the only stable 'overrange' condition permissible.

More About the Integrator, Comparator, Clock and Counters

It can be difficult to get one's head around how this dual-slope A/D converter functions, at least in any detail; here are some basic givens:

- The clock almost always runs, except for brief periods when it is inhibited. While it is running, the counter string, from the decade counters (IC16, IC13, IC10) up through the binary dividers/counters (made from three flip-flops IC8B, IC5A, IC5B) will be counting. When the count reaches 8,000, this marks the end of a cycle. Since the clock runs at 40kHz, it takes 200mS (0.2 S) per cycle, thus there are five cycles per second, meaning that five measurements of the meter's input signal are taken every second, and the display reading updates five times per second.
- Each cycle is divided into two intervals, t_1 and t_2 . t_1 is the period during which the integrator 'ramps up' (although with negative meter input signals it will actually be ramping in the negative direction), and t_2 is the period during which the integrator 'ramps down' (actually in a positive direction in the case of a negative input signal). The counter string actually resets and starts counting again at the end of t_1 (start of t_2).
- During t_1 , the integrator ramps 'up' at a rate dependent on the meter input voltage and on the integrator IC1's associated feedback component values ('R' and 'C'). Thus the rate of change of the 'up' ramp depends on the input voltage (assuming 'R' is fixed in value at the moment, i.e. the operator is not rapidly changing the range switch during a measurement cycle). Because the ongoing count began with t_2 and not with t_1 , it was already some value over 2,000 when the count began accumulating, but the count certainly ends at the end of t_1 when the count reaches 8,000. The ramp begins at 0 Volts at the start of t_1 and since the rate of increase depends on the input voltage, at the end of t_1 the ramp will be at a voltage level dependent on the input voltage being measured.
- When the count reaches 8,000 (this marks the end of one cycle and the start of the next cycle), the logic will flip to ramping 'down', and this takes place during interval t_2 . As soon as 'Ramp Down' (t2) begins, the ramp rate NOW depends on the input voltage, the value of feedback resistor 'R', and an injection of a constant current 'I_{REF}' coming from one of the two I_{REF} source circuits, + I_{REF} or - I_{REF} , depending on whether the input voltage is positive or negative and thus whether the ramp is in the positive voltage region or the negative voltage region. The math for this is a bit complicated, but ultimately, the time it takes for the ramp to 'Ramp Down' from its 'end of t_1 voltage level' back to the point where it reaches (and slightly crosses) 0 Volts, the count at the end of t_2 equals a value "N". A storage pulse generated at the end of t_2 copies the N value into the storage registers for display.
- The dynamic interaction of rates and their influences during the cycle results in the count accuracy being unaffected by the accuracy of the clock oscillator, which otherwise would be the major factor influencing A/D Conversion accuracy and stability.
- Using various tricks of signal timing during the cycle, logic can determine input polarity and 'overrange' conditions.

IM-102 (Weston 1240) Logic Block Diagram



Heathkit/Weston logic component designation Cross Reference

Note that within a given logic IC having multiple sections (e.g. *dual* F/F, *hex* inverter, etc), the section-identifying suffix (A, B, etc) is (mostly) consistent between the two brand versions, so using this table it is easy to cross reference between the logic of the two versions. Note that this table also includes the op-amps, although they are analog rather than logic, for convenience. Likewise, four transistors used in the logic section are cross referenced.

Heathkit IM-102	Weston 1240	Description	Comment
IC1	U101	Op-amp SL11862 **	
IC2	U102	Op-amp TOA8709(V)	
IC3	U103	Comparator SN72710 ***	*See also IC19/U104*
IC4	U215	Dual JK F/F MC776P	
IC5	U214	Dual D F/F MC778P	
IC6	U211	Quad NOR Gate MC724P	
IC7	U212	Quad NOR Gate MC717P	
IC8	U213	Dual D F/F MC778P	
IC9	U210	Hex inverter MC789P	
IC10	U203	Decade counter CμL9958	
IC11	U206	Buffer storage CμL9959	
IC12	U209	Display decoder/driver CμL9960	
IC13	U202	Decade counter CμL9958	
IC14	U205	Buffer storage CμL9959	
IC15	U208	Display decoder/driver CμL9960	
IC16	U201	Decade counter CμL9958	
IC17	U204	Buffer storage CμL9959	
IC18	U202	Display decoder/driver CμL9960	
IC19	U104	Op-amp TOA8709(V)	*See also IC3/U103*
Q10	Q204	NPN transistor ETS083 *	
Q11	Q203	NPN transistor ETS083 *	
Q12	Q202	NPN transistor ETS083 *	
Q13	Q201	NPN transistor ETS083 *	

Note that the Weston documentation inaccurately depicts certain logic symbols. They use the "AND" gate symbol for an actual "NOR" gate (wrong shape gate symbol and missing the inverting output circle), and a "buffer" symbol for a logic inverter (missing the inverting output circle).

** This is the manufacturer's PN used by Heathkit. The Weston uses the 2N5175 type instead.*

*** This is the manufacturer's PN used by Heathkit. The Weston uses the TIC60108V type instead.*

**** This is the manufacturer's PN used by Heathkit. The Weston uses the UA710C type instead.*